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APPLICANT: **Koichi ISHIMI**	
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
VAP		JP 6-164379	06/10/1994	PENTEL KK		(Japan w/English Abstract)	
VAP		JP 62-42613	02/24/1987	MATSUSHITA ELECTRIC IND CO LTD		(Japan w/English Abstract)	
VAP		JP 4-12842	03/05/1992	MOTOROLA, INC.	(Corresponding to WO85/02275)		
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
VAP		Kouichi Ishimi et al., "A Full-Digital PLL for Low Voltage LSIs", Technical Report of IEICE. ED97-45, SDM97-23, ICD97-35, pp. 29-36, June 1997
VAP		Michel Combes et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, pp. 956-965, July, 1996

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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